REPLACEMENT CLAIMS

Please cancel claims 1-13 without prejudice.

33. (New Claim) A method for a processor to initiate, via a coprocessor bus, execution by a coprocessor of an instruction received by the processor for execution thereby, the method comprising:

receiving said instruction;

decoding said instruction;

providing to said coprocessor, at least partially coincident with said decoding:

at least a predetermined portion of said instruction, via a first portion of said coprocessor bus, and

a first control signal indicating that said instruction is being decoded by said processor via a second portion of said coprocessor bus;

providing a second control signal to said coprocessor bus to indicate when execution of said instruction is proceeding; and

if said first control signal is negated before said second control signal is asserted, discontinuing processing of said instruction.

34. (New Claim) A method for a processor to initiate, via a coprocessor bus, execution by a coprocessor of an instruction received by the processor for execution thereby, the method comprising:

receiving said instruction;

decoding said instruction;

providing to said coprocessor, at least partially coincident with said decoding:

at least a predetermined portion of said instruction, via a first portion of said coprocessor bus, and

a first control signal indicating that said instruction is being decoded by said processor via a second portion of said coprocessor bus; and

if execution of an earlier instruction, prior to said instruction, causes an exception, negating the first control signal and discontinuing processing of said instruction.

35. (New Claim) A method for a processor to initiate, via a coprocessor bus, execution by a coprocessor of an instruction received by the processor for execution thereby, the method comprising:

receiving said instruction;

decoding said instruction;

providing to said coprocessor, at least partially coincident with said decoding:

at least a predetermined portion of said instruction, via a first portion of said coprocessor bus, and

a first control signal indicating that said instruction is being decoded by said processor via a second portion of said coprocessor bus; and

if said instruction is discarded from an instruction register within said processor, negating the first control signal and discontinuing processing of said instruction.

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36. (New Claim) A method for a processor to initiate, via a coprocessor bus, execution by a coprocessor of an instruction received by the processor for execution thereby, the method comprising:

receiving said instruction;

decoding said instruction;

providing to said coprocessor, at least partially coincident with said decoding:

at least a predetermined portion of said instruction, via a first portion of said coprocessor bus, and

a first control signal indicating that said instruction is being decoded by said processor via a second portion of said coprocessor bus; and

receiving a second control signal from said coprocessor bus, said second control signal for assisting said coprocessor to fill an instruction buffer within said coprocessor.

37. (New Claim) A method for a processor to initiate, via a coprocessor bus, execution by a coprocessor of an instruction received by the processor for execution thereby, the method comprising:

receiving said instruction;

decoding said instruction; and

providing to said coprocessor, at least partially coincident with said decoding:

at least a predetermined portion of said instruction, via a first portion of said coprocessor bus, and

a first control signal indicating whether said processor is operating in supervisor mode via a second portion of said coprocessor bus.

38. (New Claim) A method for a processor to initiate, via a coprocessor bus, execution by a coprocessor of an instruction received by the processor for execution thereby, the method comprising:

receiving said instruction;

decoding said instruction;

providing to said coprocessor, at least partially coincident with said decoding:

at least a predetermined portion of said instruction, via a first portion of said coprocessor bus, and

a first control signal indicating that said instruction is being decoded by said processor via a second portion of said coprocessor bus; and

receiving from said coprocessor, a second control signal indicating whether said predetermined portion of said instruction caused an exception within said coprocessor.

39. (New Claim) The method of claim 38, wherein the second control signal is received prior to said processor completing said instruction.

40. (New Claim) The method of claim 38, further comprising discarding said instruction.

41. (New Claim) The method of claim 40, further comprising negating the first control signal.

42. (New Claim) The method of claim 40, further comprising providing a third control signal to said coprocessor bus to indicate when execution of said instruction is proceeding, wherein if the first control signal is negated, the third control signal is not asserted.

43. (New Claim) The method of claim 38, further comprising providing a third control signal to said coprocessor bus to indicate when execution of said instruction is proceeding, wherein if the first control signal is asserted, the third control signal is asserted.

44. (New Claim) A method for a coprocessor to perform an operation in response to an instruction received by a processor coupled to said coprocessor via a coprocessor bus, the method comprising:

receiving from said processor, at least a predetermined portion of said instruction via a first portion of said coprocessor bus and a first control signal indicating that said instruction is being decoded by said processor, via a second portion of said coprocessor bus;

initiating execution of said instruction; and

providing to said processor a control signal indicating whether said instruction caused an exception.

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45. (New Claim) The method of claim 44, wherein said control signal is provided to said processor prior to said instruction completing in said processor.

46. (New Claim) A method for a processor to initiate, via a coprocessor bus, execution by a coprocessor of an instruction received by the processor for execution thereby, the method comprising:

in said processor:

receiving said instruction;

decoding said instruction; and

providing to said coprocessor, at least partially coincident with said decoding, at least a predetermined portion of said instruction, via a first portion of said coprocessor bus, and

a first control signal indicating that said instruction is being decoded by said processor via a second portion of said coprocessor bus;

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in said coprocessor:

receiving from said processor,

the predetermined portion of said instruction, via the first portion of said coprocessor bus, and

the first control signal, and

providing to said processor a second control signal indicating whether said instruction caused an exception, via a third portion of said coprocessor bus.